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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,827	11/13/2003	Jun Koyama	12732-176001	7838

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EXAMINER	
LAO, LUN YI	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/705,827	KOYAMA ET AL.	
	Examiner	Art Unit	
	LUN-YI LAO	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/24/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1- 44 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-16 of copending Application No. 10/118,917 in view of Kuwajima et al(6,339,422).

The copending application(10/118,917) teach a display comprising a first means for diving one frame period into a plurality of subframe periods and expressing n-bits gradation(n is natural number of two or more) in accordance with a total lighting time during a frame period and second means not for dividing one frame period into a plurality of subframe periods and second means for setting one of lighting and non-lighting to the one frame period, for expressing 1-bit gradation in accordance with a

total lighting time during the one frame period, and for operating the display with a lower clock frequency than the first means (see claims 1-16).

The copending application teach(10/118,917) fails to disclose second means having a lower driving voltage or current than the first means.

Kuwajima et al teach a voltage applied to the pixel element in the frame period of the first display mode is higher than in the frame period of the second display mode(see figures 2-3; column 7, lines 66-68 and column 8, lines 1-6). It would have been obvious to have modified the copending application(10/118,917) with the teaching of Kuwajima et al, since more gray scale level need more voltage.

As to claims 7, 8, 16, 26-27 and 35, it would have been obvious to have a current supplied to the pixel element in the frame period of the first display mode is larger than frame period of the second display mode since Kuwajima et al teach a voltage applied to the pixel element in the frame period of the first display mode is higher than in the frame period of the second display mode(see figures 2-3; column 7, lines 66-68 and column 8, lines 1-6) and the current will increased when the voltage is increase.

3. Claims 1-44 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-26 of copending Application No. 10/385,712 in view of Kuwajima et al(6,339,422)

The copending application(10/385,712) teaches a display comprising a first means for diving one frame period into a plurality of subframe periods and expressing

n-bits gradation(n is natural number of two or more) in accordance with a total lighting time during a frame period and second means not for dividing one frame period into a plurality of subframe periods and second means for setting one of lighting and non-lighting to the one frame period, for expressing 1-bit gradation in accordance with a total lighting time during the one frame period, and for operating the display with a lower voltage or current than the first means (see claims 1-26).

The copending application(10/385,712) fail to disclose a second manes for operating display with lower clock frequency than the first means.

Kuwajima et al teach a display disclose a second manes for operating display with lower clock frequency(70HZ) than the first means(140HZ)(see figures 2-5 and column 10, lines 10-19). It would have been obvious to have modified the copending application with the teaching of Kuwajima et al, so as to save power when the display operated in a binary display.

4. Claims 1-44 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-27 of copending Application No.11/419,345. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claim the same subject matter of a display comprising a first means for diving one frame period into a plurality of subframe periods and expressing n-bits gradation(n is natural number of two or more) in accordance with a total lighting time during a frame period and second means not for dividing one frame period into a plurality of subframe periods and second means for setting one of lighting and non-lighting to the one frame period, for expressing 1-bit

gradation in accordance with a total lighting time during the one frame period, and for operating the display with a lower clock frequency and a lower driving voltage than the first means (see claims 1-27).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

10/705,827(claim 1)	**11/419,345**
a display controller	a display controller
a first means for dividing one frame period into a plurality of subframe periods and setting one of lighting and non-lighting to each of the plurality of subframe periods, and for expressing n-bits gradation (n is a natural number of two or more) in accordance with a total lighting time during the one frame period;	the first display mode, one frame period is divided into a plurality of subframe periods, each of the plurality of subframe periods is either a lighting period or a non-lighting period, and an n-bit (where n is a natural number equal to or more than 2) gray scale is expressed by the sum total of a lighting time within the one frame period,
A second means not for dividing one frame period into a plurality of subframe periods, for setting one of lighting and non-lighting to the one frame period, for expressing 1-bit gradation in accordance with a total lighting time during the one frame period, and for operating the display with a lower clock frequency and a lower driving voltage than the first means,	the second display mode, the display is operated by a lower clock frequency and a lower driving voltage than in the first display mode, one frame period is either a lighting period or a non-lighting period, and a one-bit gray scale is expressed by the sum total of a lighting time within the one frame period,

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-8, 11-16, 19-27, 30-35 and 38-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanabe et al(US 2003/0011626) in view of Yamada et al(5,990,629).

As to claims 1-8, 11-16, 19-27, 30-35 and 38-44, Tanabe et al teach a display device comprising: a display; a display controller(30); a first means for dividing one frame period into a plurality of subframe periods(e.g. SF1-SF8) and setting one of lighting and non-lighting to each of the plurality of subframe periods(SF1-SF8); and for expressing n-bits gradation(e.g.n=8) in accordance with a total lighting time during the one frame period(see figures 1-4A; 6, 8A-8G); paragraph 7-15, 31 and 55-58); and a second means not for dividing one frame period into a plurality of subframe periods(SF1-SF8), for setting one of lighting and non-lighting to the one frame period, for expressing 1-bit gradation in accordance with a total lighting time during the one frame period, and for operating the display with a lower clock frequency and than the

first means, wherein the first and second means are controlled by the display controller(see figures 2, 4B, 6, 8H and paragraphs 31. 40, 64 and 65).

Tanabe et al fail to point out a display having a lower level of driving voltage.

Yamada et al teach a display device a lower driving voltage(e.g. V1)((see figures 26-29; column 37, lines 31-68 and column 38, lines 1-46). It would have been obvious to have modified Tanabe et al with the teaching of Yamada et al, so as to having a display having a lower gradation and reduce power consumption.

As to claims 3-4, 14, 22, 23 and 33, Tanabe et al as modified teach a display device further comprises a frame memory(24), n-bits data (n is natural number of two or more; e.g. n=8) is written and read out so that display is conducted in the a first means(256 level gray-scale mode) and 1-bit data is written and read out so that display is conducted in the second means(see figures 2-4B; paragraphs 31, 40, 54-58 and 64-65).

As to claims 5, 6, 11, 12, 15, 19, 24-25, 30-31, 34 and 38, Tanabe et al as Modified teach a voltage(e.g. high voltage) applied to the pixel element in the first means is higher than in the second means(0V)(see Tanabe et al's figures 2-4B; paragraphs 53-54 and 63-65; and Yamada's figures 26-29).

As to claims 7-8, 16, 26-27 and 35, Tanabe et al as modified teach a current supplied to the pixel element in the frame period of the first means is larger than the second means(see Tanabe et al's figures 2-4B; paragraph 65; Yamada's figures 26-29; column 37, lines 31-42 and column

38, lines 2-8).

As to claims 39-44, Tanabe et al teach a portable information terminal(Plasma or EL display)(see figure 2 and paragraphs 4 and 22).

7. Claims 9-10, 17-18, 28-29 and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanabe et al(US 2003/0011626) in view of Yamada et al(5,990,629) and Okuda(6,380,689).

As to claims 9-10, 17, 18, 28-29 and 36-37, Yamada et al teach the frame period is composed of two periods of a wiring period(Tadd), a display period(T_E)(see figures 23, 27 and column 39, lines 15-20).

Tanabe et al as modified fail to disclose an erasing period.

Okuda teaches a frame period comprising three periods of writing period(address period); a display period(emission period) and an erasing period(reset period)(see figures 4, 7-8 and column 4, lines 48-53). It would have been obvious to have modified Tanabe et al as modified with the teaching of Okuda, so as to clear previous display images.

Response to Arguments

8. Applicant's arguments filed on July 24, 2006 have been fully considered but they are not persuasive.

Applicants argue that Tanabe et al and Yamada et al do not teach a second means for operating the display with a lower clock frequency than the first means on

page 2-4. The examiner disagrees with that since Tanabe et al teach a second means operating the display with a lower clock frequency than the first means since a second means(see figure 4B) only need to scan row lines(A1-An) once in one field period and apply one bit data on column lines(B1-Bm) once in one field period, but a first means(first means) need to scan row lines(A1-An) eight times in the same one field period and apply four bit data on column lines(B1-Bm) eight times in the same one field period(see figures 4A, 4B, 6 and paragraph 65) and it is inherent the Tanabe's display having a clock signal since a display needs timing or timing alignment(see Yamada's figures 1, 5 and column 10, lines 43-65).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tamura(US 20030112257) teaches a displaying a low clock signal in a lower gradation display.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lun-yi Lao whose telephone number is 571-272-7671. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 4, 2007

Lun-yi Lao
Primary Examiner